POWER-ON SEQUENCING FOR LIQUID CRYSTAL DISPLAYS; WHY, WHEN, AND HOW

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ABSTRACT

Liquid Crystal Displays require special considerations upon power-up. The following explains why power-up sequencing is necessary, the required timing of the power-up sequence, and circuitry necessary to accomplish proper power-up sequencing. Each LCD display technology is discussed individually.

INTRODUCTION

Liquid crystal displays are being used more often as the display of choice in computer applications, most notably in laptop, notebook, and pen based computers. These displays are popular because they are reliable, power efficient, compact, light weight, and easily installed in hardware. Currently, one of the most overlooked design considerations is the required power on sequencing. Liquid crystal displays vary from simple one line monochrome units, up to full page graphic displays having both monochrome and color formats. This paper will discuss the reason power-up sequencing is necessary, ways to accomplish the required sequencing in both passive and active matrix displays, and provide examples of circuitry to power up and down the display properly.

POWER-ON SEQUENCING IS NECESSARY

Power-on sequencing is required mainly to protect the liquid crystal from exposure to any DC voltage. What needs to be accomplished upon powering up the display is that the 5 V must be started first. This allows the onboard logic to become active and starts an internal clock (the M clock) which sets up an AC wave form on the display electrodes. Even with very short intervals of exposure to VEE, without the "M" clock started first, the liquid crystal will begin to break down and change state. This change of state manifests itself as a change in color of the liquid crystal and eventually, the formation of gas bubbles. When this happens, the damage is permanent and the display will eventually be rendered useless. This AC wave form, the "M" clock, is controlled using a phase lock loop circuit. When VCC is started, this clock begins oscillating and resonates between VCC and VEE. As the voltage for VEE is increased, the display gains contrast. The contrast on the display is optimized by adjusting VEE.

After VCC has stabilized, the external clock and data signals should be introduced to the display module. After the clock and data signals are stable, VEE can be turned on. One word of caution, if you are using a display panel with display enable, there is a time limit as to how long the display can be function without VEE. For intervals longer than 20 ms, the display logic may latch up thus requiring a full reset. In order to fully understand the reasons for a specific power-up sequence, each display type will be discussed and the sequencing requirements for that display will be fully explained.

CHARACTER MODULE

Sharp manufactures a line of Dot Matrix Character Modules including 16 x 1; 16 x 2; 20 x 2; and 40 x 2 displays. Because these displays operate from a single power supply, power-up sequencing is not as critical as in other units. However, care must be taken to insure that the power supply is up to at least 4.5 V within 10 ms of turn on. If the display has not reached this level prior to latching the internal reset, the reset circuit will not operate normally and may latch up the display. Also, if power is interrupted, the display power must be held off for at least 1 ms prior to reapplying power or the display may once again latch up due to failure to trigger the internal reset circuit (Figure 1).

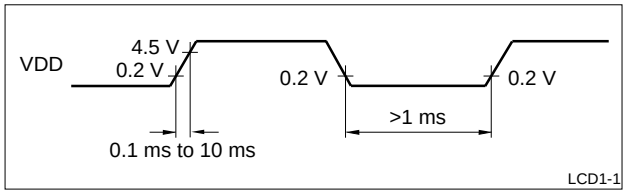


Fig. 1. Power-up Sequencing for Character Modules

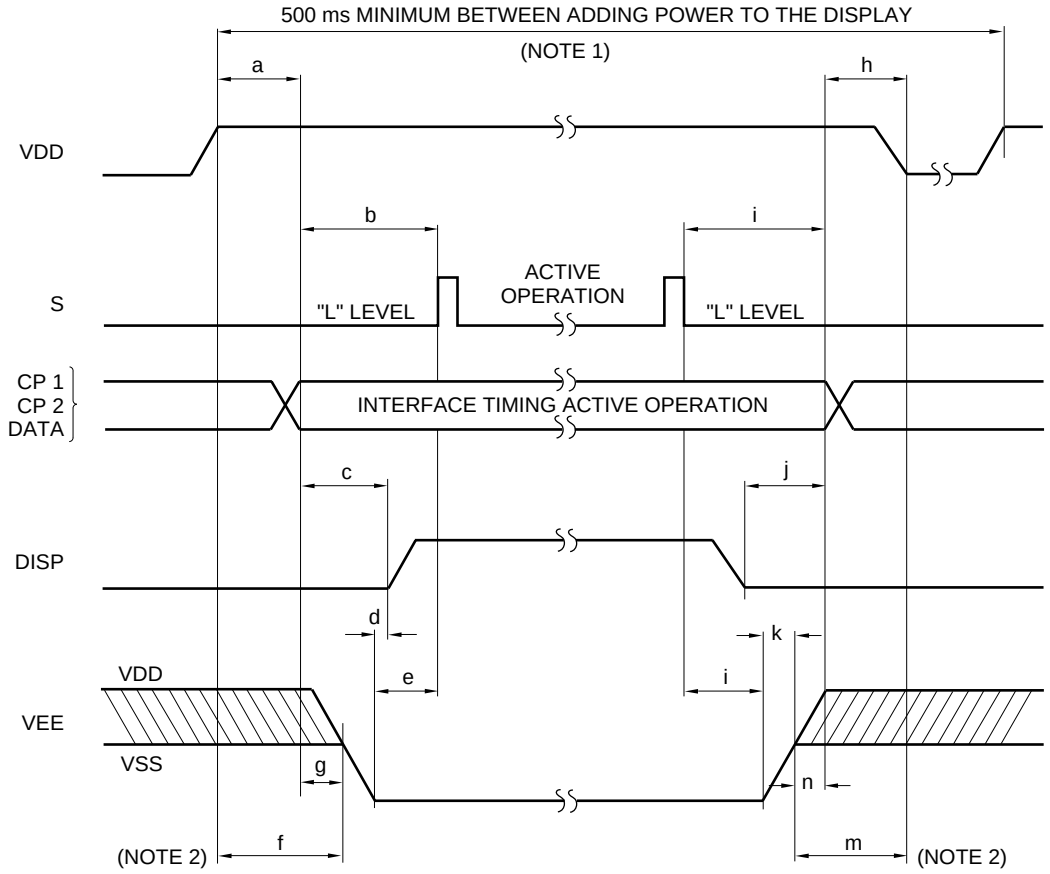
Upon power-up, you must reset the display in software. Instructions as to how to accomplish this are published in the Sharp "Display Unit Users Manual for Dot Matrix LCD Units with Built in Controllers."

PASSIVE DISPLAYS

Large area passive displays, both Monochrome and Color, require care in implementing the power-up sequencing of thedisplay. Bec ause the operating voltage of the display is higher than the DC breakdown voltage of the fluid, care must be taken to provide protection for the liquid crystal fluid. The objective of the power-up sequencing procedure is to start an internal clock, the "M" clock, and to insure stable operation of the CMOS circuitry by applying VDD prior to introduction of the logic signals. By following the recommended start up procedure, we can prevent the device inputs from being subjected to voltages greater than +0.2 VDC above VDD. If the logic is allowed to be exposed to voltages exceeding VDD +0.2 V, noise will disperse through the drivers and possibly cause lockup of the logic.

The "M" clock sets up an AC wave form which prevents DC current from flowing through the Liquid Crystal. According to the fluid manufacturer, DC voltages as low as 25 mV for even short periods of time will cause a breakdown of the liquid crystal material and eventually render the display useless. The recommendations outlined in the attached timing diagram will assure the user that the display will be fully protected from damage and premature failure.

Display Types which use the above power sequencing are: LM64P70 Series; LM64P80 Series; and the LM64C031 as well as the older Passive Matrix Displays. (Figure 2)



NOTES:

1. If during the power up sequence, the power is interrupted to the display, power must remain off for at least 500 ms, measured from the original initialization of VDD, or damage may occur to the display drivers. This time interval is necessary to allow the CMOS logic to return to a ground potential and stabilize prior to restarting the logic.
2. VEE can be at either VDD or VSS prior to turn on. If display enable is not used, then VEE must be at VDD until activation. This allows the pull up attached to display enable to hold the panel reset until activation of VEE. This will prevent the display from latching up.

LCD1-2

Fig. 2. Power-up Sequencing for Passive Displays

Table 1. Power-up Sequencing for Passive Displays

POWER ON			POWER OFF		
SYMBOL	WITH DISPLAY ENABLE	WITHOUT DISPLAY ENABLE	SYMBOL	WITH DISPLAY ENABLE	WITHOUT DISPLAY ENABLE
a	0 ms MIN	0 ms MIN. 20 ms MAX.	h	0 ms MIN.	0 ms MIN. 20 ms MAX.
b	0 ms MIN	20 ms MIN.	i	0 ms MIN.	20 ms MIN.
c	20 ms MIN	—	j	20 ms MIN.	—
d	0 ms MIN	—	k	0 ms MIN.	—
e	—	0 ms MIN.	l	—	0 ms MIN.
f	0 ms MIN	—	m	0 ms MIN.	—
g	—	0 ms MIN. 100 ms MAX.	n	—	100 ms MIN.

ACTIVE MATRIX DISPLAYS

Sharp Electronics is presently involved in manufacturing Thin Film Transistor (TFT) Active Matrix LCDs for use in Office Automation Applications and Audio Visual Applications. Each of these technologies require specific power-up sequencing to insure reliable operation of the displays. The following summarizes those requirements.

Small TFT Audio Visual Displays

Small TFT audio visual displays include the LQ4xxxx and LQ6xxxx displays. These displays, like the Passive units are susceptible to the introduction of the negative voltage (VSL) prior to initializing the logic voltage (VSH). The following diagram graphically represents the necessary timing considerations for these modules. (Figure 3)

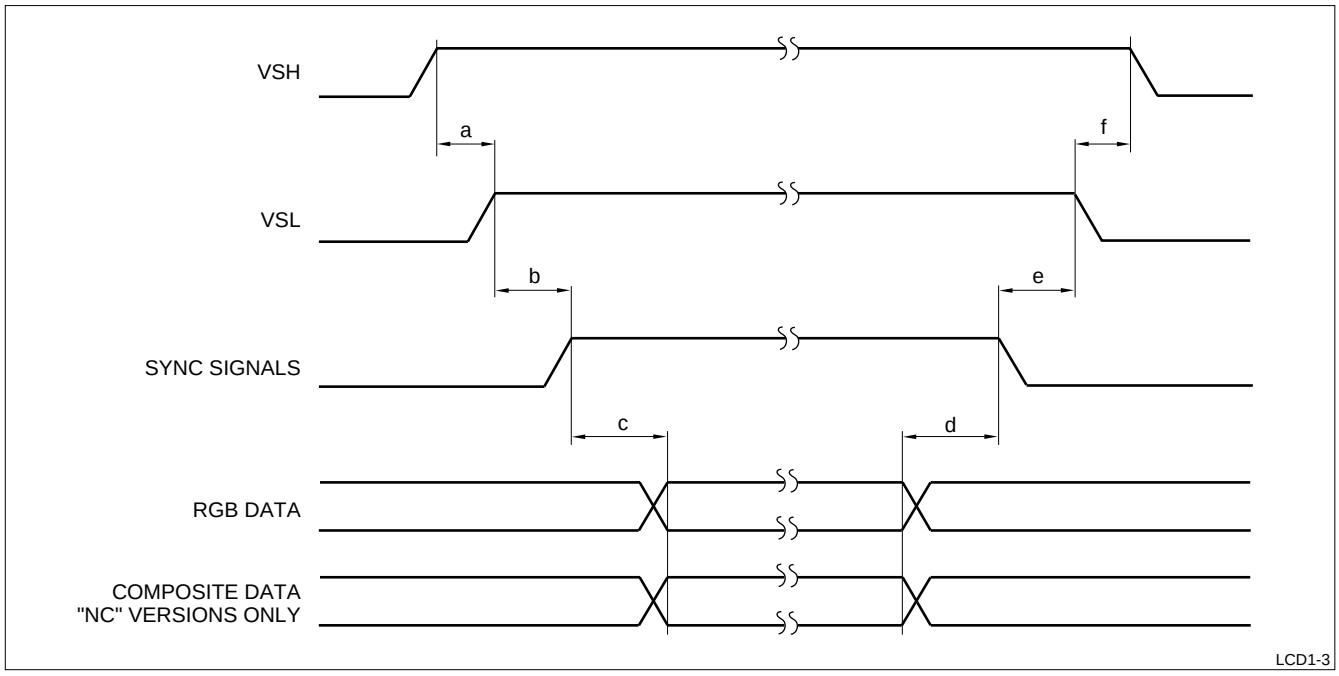


Fig. 3. Power-up Sequencing for Audio Visual TFT Displays

Table 2. Power-up Sequencing for Audio Visual TFT Displays

POWER ON			POWER OFF		
SYMBOL	MINIMUM	MAXIMUM	SYMBOL	MINIMUM	MAXIMUM
a	0 ms	100 ms	d	0 ms	20 ms
b	2 ms	20 ms	e	0 ms	20 ms
c	0 ms	20 ms	f	0 ms	100 ms

TFT Displays Without Controllers

In addition to the above mentioned audio visual displays, Sharp has a few "Special Application" displays such as the LQ323Y11 which do not come with a display controller. What makes these displays unique is that separate voltages are required for the source and gate drivers. In all instances, the "High" level voltages should be started prior to the "Low" level voltages. This means that VSH (+5 V typ.) and VGH (+13 V typ.) should be started prior to VSL (-8 V typ.) and VGL (-20 V typ.). The minimum and maximum timing requirements specified above can be used for the TFT displays without controllers by applying the standard for VSH in the table to VSH and VGH on the display and the standard for VSL in the table to VSL and VGL on the display. All other timing for the display will also be as represented in the table.

Large TFT Office Automation Displays

The original offering in office automation products were the LQ10 and 011 products. These displays require multiple power supply inputs of +5 VDC at 0.45 watts and +12 VDC at 4.68 watts. As with other displays, it is necessary to power up the displays in the proper sequence to prevent latch up of the display logic. Latch up of the display causes a failure of the "M" clock to start and subjects the liquid crystal to DC Voltages. If latch up occurs, the liquid crystal itself will be electrochemically decomposed thus permanently damaging the display. The timing diagram (Figure 4) must be implemented in order to assure that the display will not be damaged.

The newest offering in large format TFT displays is the LQ9D011. With this display, there is a requirement for only one power supply. Resident circuitry divides the single supply into the various voltages required by the panel. The only requirement for this display is that the power must be present prior to, or simultaneously with the input signals. If not, the display may latch up. The circuit used for the LQ10 TFTs should be implemented on the LQ9 display, to supply power when the input signals are present, and to remove power if the HSYNC or CLK are interrupted. Because of the display configuration it will only be necessary to connect VDD in Figure 5 to the +5 V input on the display. The +12 V is not necessary on the LQ9 displays.

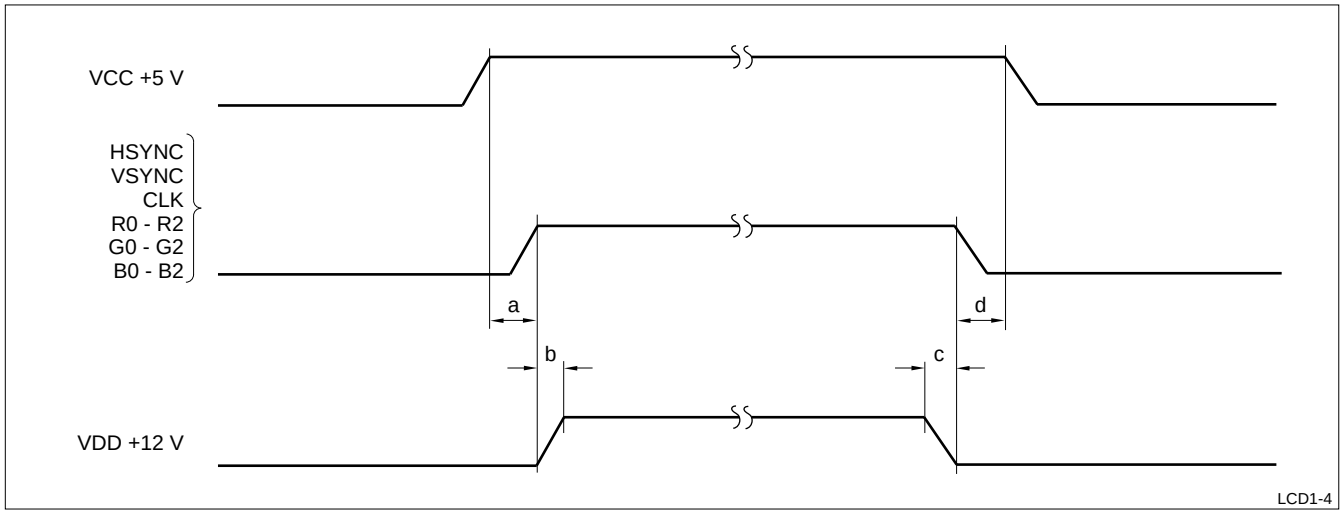


Fig. 4. Power-up Sequencing for LQ10xxxx Office Automation Displays

Table 3. Power-up Sequencing for LQ10xxxx Office Automation Displays

POWER ON			POWER OFF		
SYMBOL	MINIMUM	MAXIMUM	SYMBOL	MINIMUM	MAXIMUM
a	0 ms	100 ms	c	0 ms	20 ms
b	2 ms	20 ms	d	0 ms	100 ms

Power-on Sequencing Circuitry

The following circuit (Figure 5) is set up to sequence the power supply on the Sharp LQ10D011 display. The circuit senses clock and horizontal sync, energizes the power supplies whenever these signals are present. If for any reason the HSYNC or CLK signals are interrupted, the relay will open thus interrupting VDD and VEE to the display. This will prevent any possibility of damaging the display. The circuit is set up to open the power supply line if the signals are lost for more than 28 ms. The power will be restored if the two signals return.

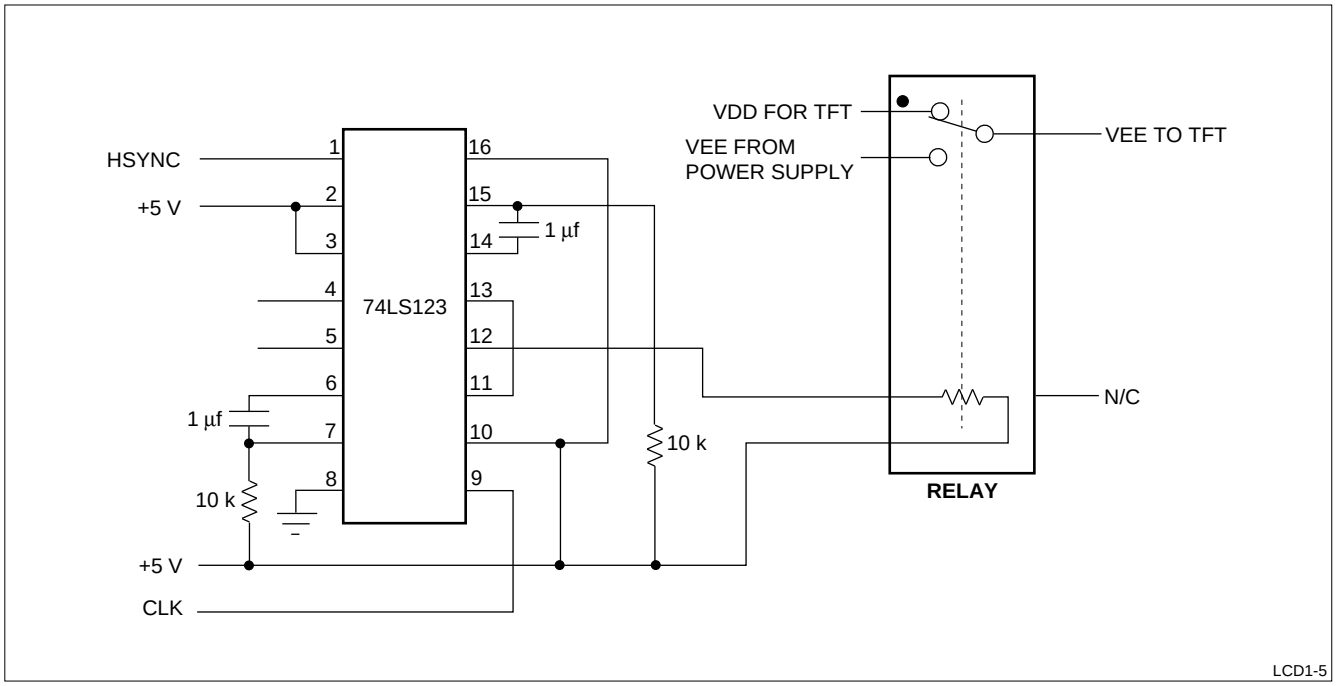


Fig. 5. Power Supply Sequencing Circuit for LQ10xxxx TFT Displays

Power Supply Sequencing for Passive Displays

Figure 6 is set up to sequence the power supply on the Sharp passive displays including monochrome displays and the LM64C031 passive color display. The circuit senses upper and lower data clocks and energizes the power supplies whenever these signals are present. If for any reason the clock signals are interrupted, the relay will open thus interrupting VDD and VEE to the display. This will prevent any possibility of damaging the display through the introduction of Direct Current to the liquid crystal material. The circuit is set up to open the power supply line if the signals are lost for more than 28 ms. The power will be restored if the two signals return.

NEW GENERATION CONTROLLERS

Chips and Technologies Controllers

The new generation controllers include signals specifically to control the sequencing of the display power. In their new Vampire board with the 65520/530 chip set, Chips & Technologies supplies ENAVDD and ENAVEE signals to control the VDD and VEE voltages respectively. The signals are intended to be control lines which drive external power devices sized to handle the required current. Figure 7 is a diagram of the required circuitry and the timing provided by the controller. A contrast adjustment circuit is illustrated in the Chips and Technology literature and may be added to this circuit diagram as required. The contrast circuit has been removed from this example for clarity.

In the 65520, the timing for VDD and VEE on and off is fixed, however, in the 65530, the timing is programmable using the POWER SEQUENCING DELAY REGISTER (XR5B). The power-on delay time in the 65520 is set at 32 ms for each interval, a, b, c, & d. In the 65530, the interval default is 32 ms, however, the delay may be programmed up to 60 ms in 4 ms intervals on the power-up cycle, and up to 480 ms in 32 ms intervals on the power-down mode. (Figure 8)

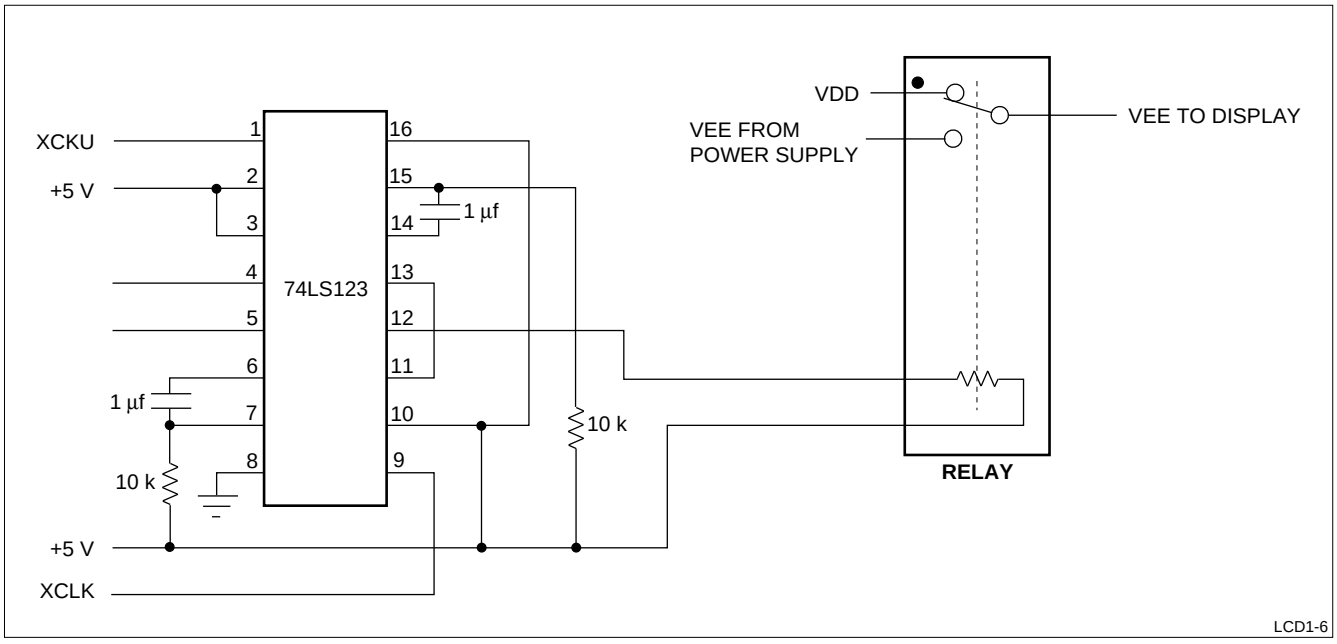


Fig. 6. Power Supply Sequencing Circuit for Passive Displays

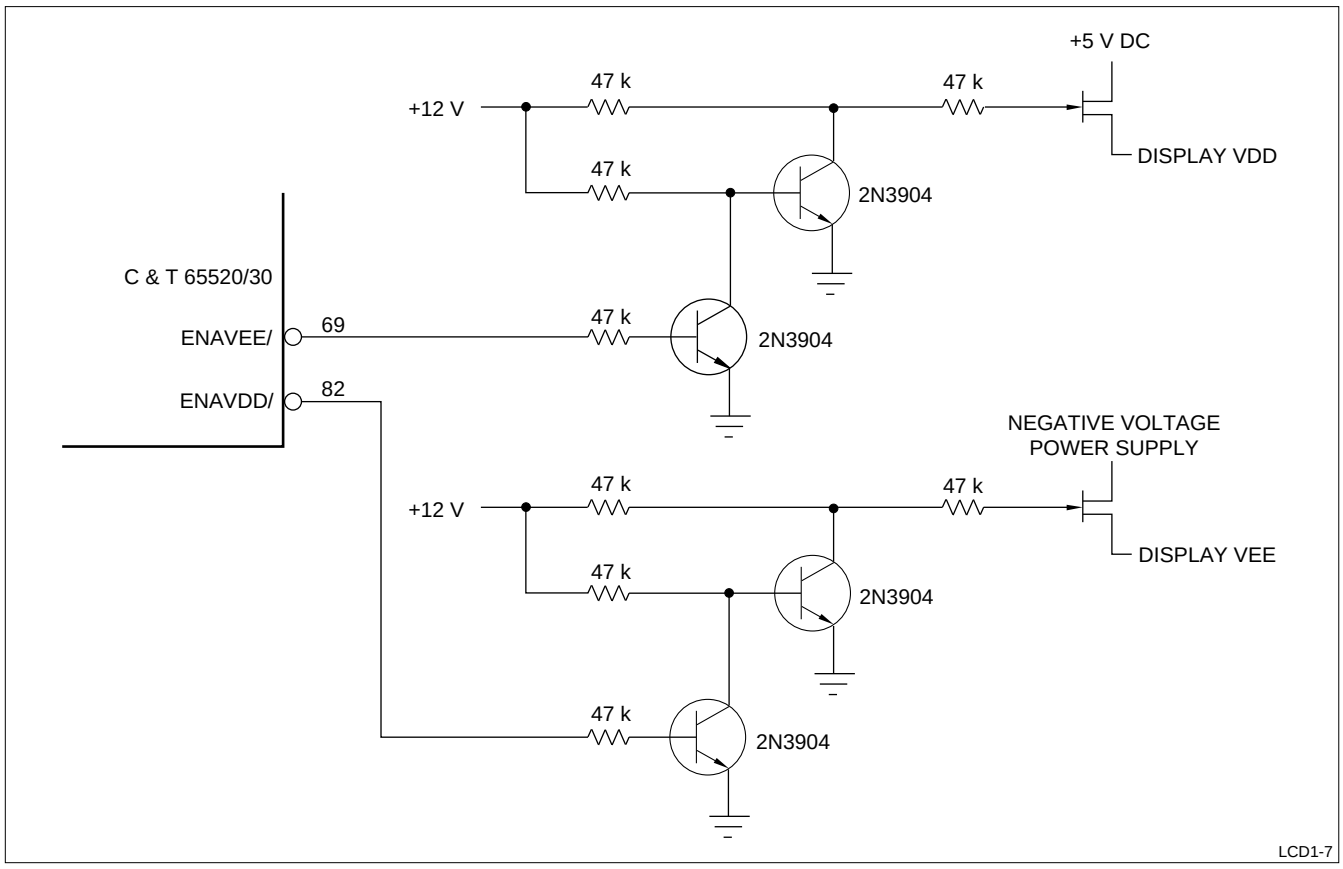


Fig. 7. Chips and Technology Power-up Sequencing Circuit 65520/30 Demo Board

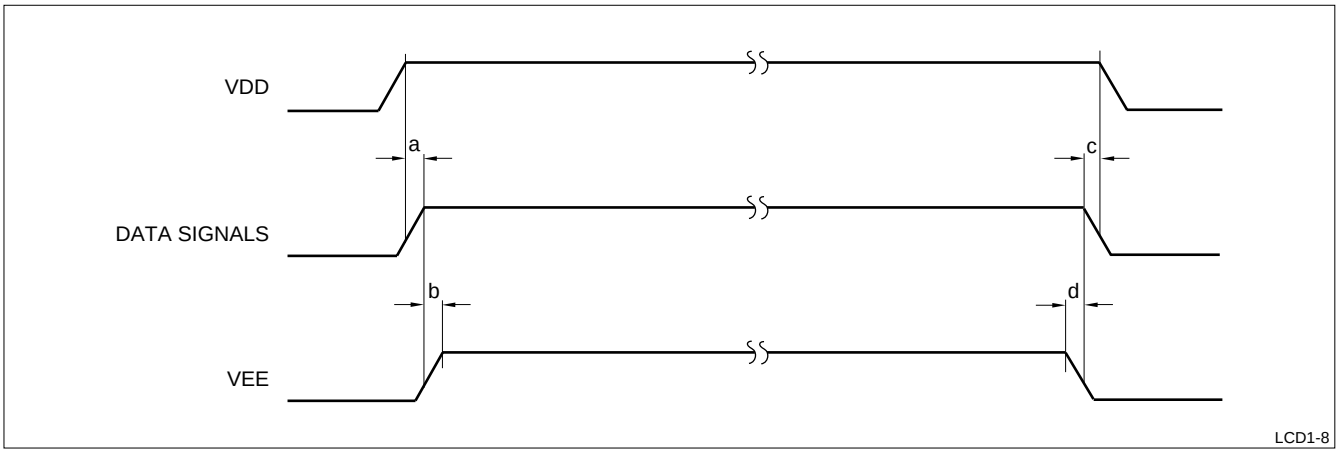


Fig. 8. Chips and Technology Power-up Sequencing Circuit 65520/30 Demo Board

Cirrus Logic Controllers

Cirrus Logic also supplies FPVCC and FPVEE signals from their GD6340 controller. The controller manages the power up/down sequencing completely. The only additional components necessary are the actual power devices as illustrated in Figure 9, and are sized to handle the required current.

The Cirrus Logic GD6340 has logic to correctly sequence the power-on and off in LCD applications. The FPVCC and FPVEE pins are simply CMOS outputs which supply control signals intended to drive external power management components. Sample circuitry used to accomplish the proper power management is illustrated in Figure 9. A contrast control circuit may be added to the above circuitry. Please refer to the Cirrus Logic documentation for recommended schematics for this circuit. The timing (Figure 10) for intervals a, b, c, and d, are all set at 37 ms in the Cirrus Logic controller.

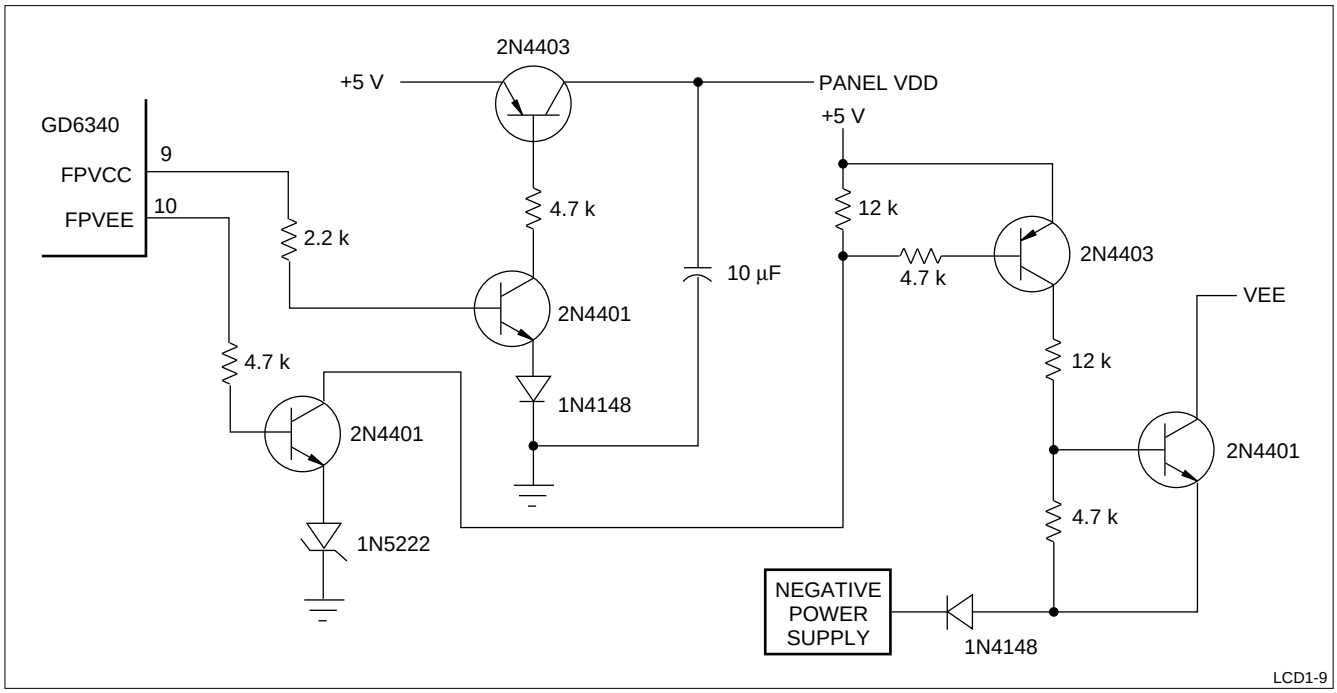


Fig. 9. Cirrus Logic Power-up Sequencing Circuit GD6340 Demo Board

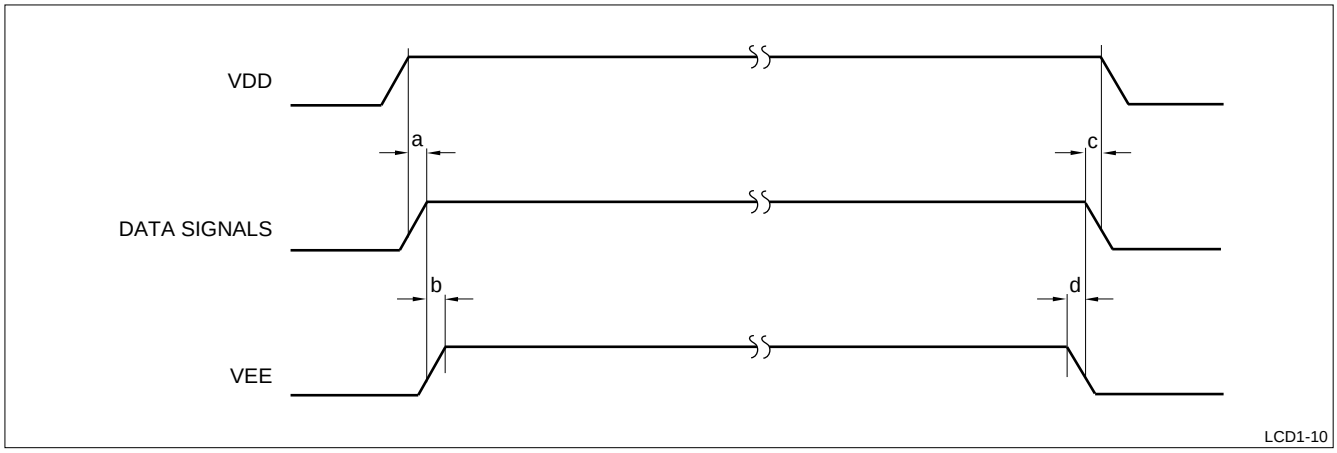


Fig. 10. Timing for Cirrus Logic GD6340 Power-up Sequencing

Western Digital Controllers

Within the Western Digital chip set, there is a signal (LCDN) dedicated to controlling the Power-on/off sequencing for the LCD. In their demonstration board, the signal is routed through the circuit (Figure 11) to enable control of power initialization and to delay the removal of power until the logic signals have been turned off. The intervals a, b, c, and d, are set to be approximately 30 ms (Figure 12). Contrast adjustment can be added to the circuit.

CONCLUSIONS

Power-up sequencing of Liquid Crystal Displays is critical. This application noteis intended to express the importance of this function and to make suggestions as to the required implementation. All of the major controller chip manufacturers have recognized the importance of this feature and have implemented logic to assist the designer in incorporating this feature into his hardware.

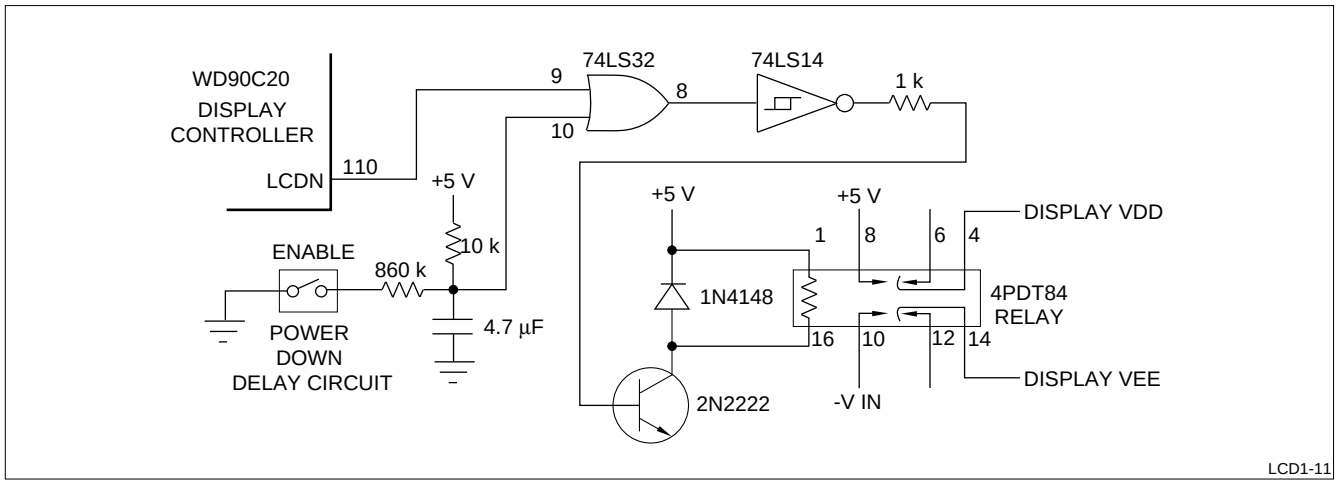


Fig. 11. Western Digital Power-up Sequencing Circuit WD90C20 Demo Board

Fig. 12. Timing for Western Digital WD90C2X Power-up Sequencing

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